REMARKS

Status of the Claims

Claims 1-64 were previously canceled. Claims 65-150 were added by the amendment presented on February 26, 2010. Although the present action regards the Applicant's February 26, 2010 response as "non-compliant," the Examiner acknowledged Applicant's amendments in that response. Applicant presumes that the current status of the claims is as stated in their February 26, 2010 response. In this response, Applicant makes further amendments in this context. Specifically, in this response claim 65 is amended and claims 108-123 have been canceled without prejudice to the subject matter therein.

Response to Election/Restrictions

The Examiner contends that the amendment filed February 26, 2010 is nonresponsive in that, in the Examiner's view, claims drawn to an elected invention were canceled and claims drawn to a non-elected invention were added. The Examiner contends that canceled claims 1-64 appear to be related to the embodiment of FIG. 6, and that new claims 65-150 appear to be directed to the embodiment of FIG. 8. Applicant traverses with respect to the pending claims for the reasons set forth below.

Figures 6 and 8 are reproduced below for ease of reference:

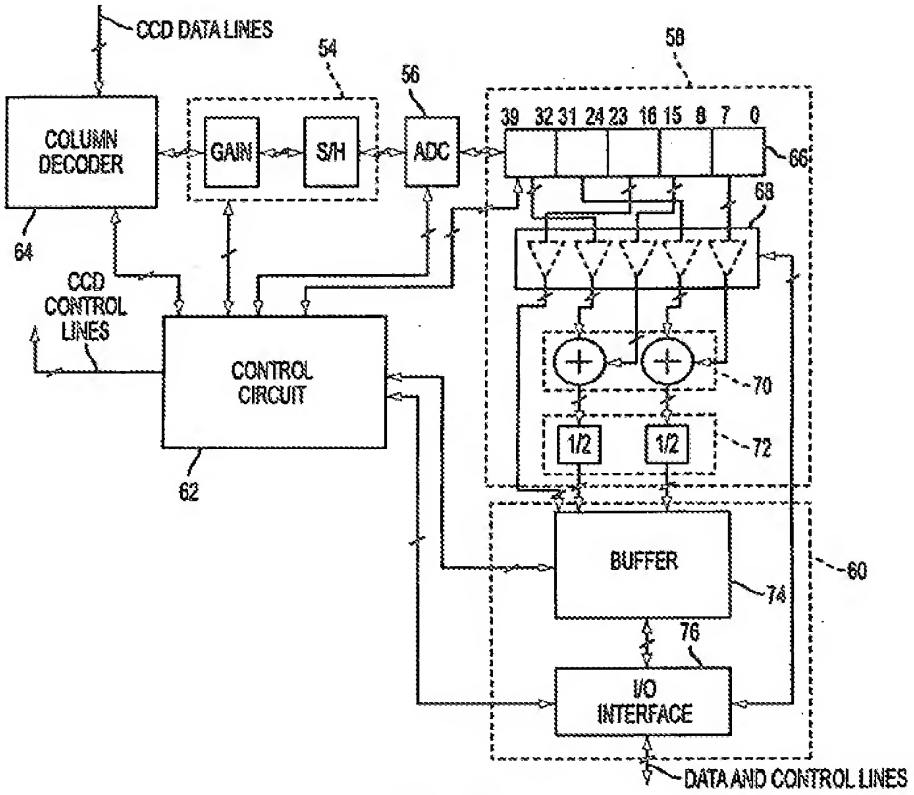
CCD DATA LINES
54
56
58
COLUMN DECODER
GAIN
S/H
ADC
39 32 31 24 23 16 15 8 7 0
66
68
64
CCD CONTROL LINES
CONTROL CIRCUIT
70
1/2
1/2
72
62
BUFFER
74
60
76
I/O INTERFACE
DATA AND CONTROL LINES

FIG. 6

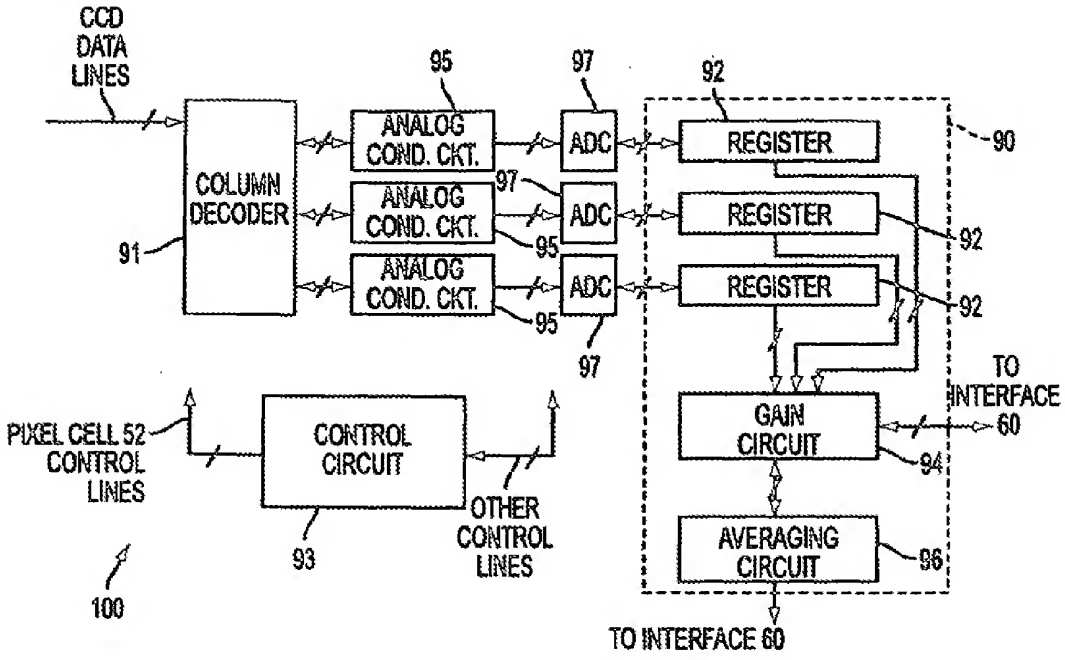
CCD DATA LINES
95
97
92
ANALOG COND. CKT.
ADC
REGISTER
90
COLUMN DECODER
97
ANALOG COND. CKT.
ADC
REGISTER
92
91
95
ANALOG COND. CKT.
ADC
REGISTER
92
95
97
TO INTERFACE 60
GAIN CIRCUIT
94
PIXEL CELL 52 CONTROL LINES
CONTROL CIRCUIT
OTHER CONTROL LINES
93
AVERAGING CIRCUIT
96
100
TO INTERFACE 60

FIG. 8

For at least the reasons set forth in the tables below, Applicant submits that independent claims 65 (as amended), 81, 93, 124 and 136 are generic in that they read upon both Figure 6 and Figure 8. The currently pending claims therefore read on the elected inventions because, as illustrated in the tables below, the claims are still related to the FIG. 6 embodiment. The amended claims are related to additional embodiments (i.e., FIG. 8 in addition to FIG. 6) but not solely to a different embodiment. Applicant requests reconsideration and withdrawal of the restriction requirement, and rejoinder of all pending claims.

Claim 65	**FIG. 6**	**FIG. 8**
65. (Currently amended) A CMOS imager comprising: an array of pixels, disposed on a semiconductor substrate, including a red pixel to provide a red pixel signal to indicate an amount of red light sensed by the red pixel, a green pixel to provide a green pixel signal to indicate an amount of green light sensed by the green pixel, and a blue pixel to provide a blue pixel signal to indicate an amount of blue light sensed by the blue pixel;	**"array of pixels"**: Implied by the "CCD Data Lines" input. See also FIG. 5 and related text.	Same as FIG. 6.
an interpolator, disposed on the semiconductor substrate, to receive pixel signals corresponding to groups of pixels of the array, including, for at least one of the groups, a first number of rows of pixels and at least the first number of columns of pixels, and to estimate an amount of green and blue light received by the red pixel using at least the green and blue pixel signals, an amount of red and blue light received by the green pixel using at least the red and blue pixel signals, and an amount of red and green light received by the blue pixel using at least the red and green pixel signals;	**"an interpolator"**: item 58 **"to receive pixel signals"**: from CCD data lines, through circuitry 54 and ADC 56. **"corresponding to groups of pixels of the array"**: bits 0-39 of register 66 correspond to pixel cells 52 (see [0034]). **"a first number of rows of pixels"**: one	**"an interpolator"**: item 90 **"to receive pixel signals"**: from CCD data lines, through column decoder 91, analog conditioning circuits 95 and ADCs 97. **"corresponding to groups of pixels of the array"**: "Similar to the register 66" (see [0038]), register 92 contains digital representations of

	row (see [0034]) **"at least the first number of columns of pixels"**: at least one column (see [0034]) **"estimate an amount"** of light: by operation of interpolator 58. See also [0035].	five adjacent pixel cells 52. **"a first number of rows of pixels"**: one row, repeated 3 times. See [0038] **"at least the first number of columns of pixels"**: at least one column (see [0038]) **"estimate an amount"** of light: by operation of interpolator 90. See also [0038].
at least the first number of analog-to-digital converters, disposed on the semiconductor substrate, coupled to receive pixel signals from the array, to convert the red, green, and blue pixel signals from analog to digital signals, wherein the first number is at least ~~three~~ one;	**"at least the first number"** of A/D converters: first number = 1 **"coupled to receive pixel signals from the array"**: from CCD data lines, through circuitry 54.	**"at least the first number"** of A/D converters: first number = 3. **"coupled to receive pixel signals from the array"**: from CCD data lines, through column decoder 91, and analog conditioning circuits 95.
a register set, disposed on the semiconductor substrate, that is programmable via an external interface, wherein the interpolator is to operate depending on one or more values to be stored in the register set; and	**"a register set"**: 5-stage serial registers 66. **"an external interface"**: control circuit 62 **"one or more values to be stored in the register set"**: See [0035]: "The interpolator **58** assigns a weight via scalar multipliers to the values represented by the bits 32-39 and 8-15 of the register **66**."	**"a register set"**: 5-stage registers 92. **"an external interface"**: control circuit 93 **"one or more values to be stored in the register set"**: See [0038]: "Each register **92** has representations from the same column of pixel cells **52**."
a parallel port interface, external to the imager, to provide output signals associated with the red, green, and blue pixel signals.	**"a parallel port interface"**: parallel port interface **60** shown in FIG. 6.	**"a parallel port interface"**: gain circuit 94 and averaging circuit 96, both within interpolator 90, have connections to "interface 60."

Claim 81	FIG. 6	FIG. 8
81. (Previously presented) A CMOS imager comprising: an array of pixels, disposed on a semiconductor substrate, including a red pixel to provide a red pixel signal to indicate an amount of red light sensed by the red pixel, a green pixel to provide a green pixel signal to indicate an amount of green light sensed by the green pixel, and a blue pixel to provide a blue pixel signal to indicate an amount of blue light sensed by the blue pixel;	**"array of pixels"**: See claim 65	**"array of pixels"**: See claim 65
an interpolator, disposed on the semiconductor substrate, to receive a group of pixel signals associated with a group of pixels of the array having M rows of pixels and N columns of pixels, the interpolator to estimate an amount of light of first and second colors, received but not sensed by a target pixel, using selected pixel signals within the group of pixel signals associated with pixels that sense light of the first and second colors;	See claim 65. M= 1; and N= 5.	See claim 65. M= 3; and N= 5.
at least M analog processing circuits, disposed on the semiconductor substrate, coupled to receive pixel signals from the array, each of the analog processing circuits comprising respective circuitry to perform correlated double sampling and analog-to-digital conversion, wherein each of the analog processing circuits is coupled to a respective one of at least M signal lines from a column decoder;	**"analog processing circuit"**: analog conditioning circuitry 54 and ADC 56.	**"analog processing circuit"**: analog conditioning circuitry 95 and ADC 97
a writable and readable register set, disposed on the semiconductor substrate, accessible via an external interface, to store at least one value to affect an output of interpolated pixel signals; and	**"a writable and readable register set"**: 5-stage serial registers 66. **"accessible via an external interface"**: reads data from CCD data lines, and outputs data through scalar multipliers 68. **"to affect an output of interpolated pixel signals"**: register contents are used to interpolate color	**"a writable and readable register set"**: 5-stage registers 92. **"accessible via an external interface"**: reads data from CCD data lines, and outputs data through gain circuit 94. **"to affect an output of interpolated pixel signals"**: register contents are used to interpolate color values for adjacent

	values for adjacent pixels (see [0035]).	pixels (see [0038]).
an external data output port, to provide first output signals associated with the red, green, and blue pixel signals, and, in accordance with the at least one value to be stored in the register set, to further provide second output signals associated with the amount of light of the first and second colors estimated by the interpolator to be received but not sensed by the target pixel.	**"an external data output port"**: parallel port interface **60** shown in FIG. 6. **"first output signals"**: The directly-measured color intensity for each pixel. See [0031]: "The processing of a given photosensitive site 51 includes retrieving the color level sensed by the pixel cell 52 of the given photosensitive site 51 and estimating the missing color levels." **"second output signals"**: The *estimated* color level of the missing colors for each pixel. See [0031]: "The interpolator 58 estimates the levels of the missing color levels for a given photosensitive site 51 using the outputs of other pixel cells 52 that are close to the given photosensitive site 51."	**"an external data output port"**: gain circuit 94 and averaging circuit 96, both within interpolator 90, have connections to "interface 60." **"first output signals"**: The directly-measured color intensity for each pixel. **"second output signals"**: The *estimated* color level of the missing colors for each pixel. See [0038]: "the outputs from pixel cells 52 from more than one row are used to estimate the missing color levels of a photosensitive site 51."

Claim 93	**FIG. 6**	**FIG. 8**
93. (Previously presented) A system comprising: a writable and readable register set disposed on a semiconductor substrate and coupled via an external input-output port to an external programming interface, the register set storing a value written to the register set via the programming interface;	**"a writable and readable register set"**: Within I/O Interface 76. See [0037]. **"coupled via an external input-output port"**: Control circuit 62	**"a writable and readable register set"**: Within I/O Interface 76, which is part of interface 60. See [0037]. **"coupled via an external input-output port"**: Control

	and/or I/O Interface 76. **to an external programming interface**": Gains of the scalar multipliers 68 are programmable through I/O Interface 76 (see [0037]). **"the register set storing a value written to the register set via the programming interface"**: The registers of I/O Interface 76 store multiplier gain values. See [0037].	circuit 93 and/or "to interface 60" at lower right of FIG. 8, which includes I/O Interface 76. **to an external programming interface"**: Gains of the scalar multipliers 68 are programmable through I/O Interface 76 (see [0037]). **"the register set storing a value written to the register set via the programming interface"**: The registers of I/O Interface 76 store multiplier gain values. See [0037].
an array of photodiodes, disposed on the semiconductor substrate, including a first photodiode to provide a first signal to indicate an amount of red light sensed by the first photodiode, and a second photodiode to provide a second signal to indicate an amount of blue light sensed by the second photodiode;	**"an array of photodiodes"**: Implied by the "CCD Data Lines" input. See also FIG. 5 and related text.	Same as FIG. 6.
an estimation circuit, disposed on the semiconductor substrate, to receive a group of signals associated with a group of photodiodes of the array and to use the group of signals to estimate an amount of red and blue light received by a pixel having a photodiode configured to sense green light, wherein the group of signals are associated with photodiodes that sense red and blue light, the estimation circuit to provide first and second estimated signals to indicate the amount of the red and blue light, respectively, estimated by the estimation circuit to be received by the pixel; and	**"an estimation circuit"**: interpolator 58. The recited operation using interpolator 58 is described at least at [0031], [0034] and [0035].	**"an estimation circuit"**: interpolator 90. The recited operation using interpolator 90 is described at least at [0038].
an external data output port from which to read out the first output signals associated with the first and second signals that indicate the amount of red and blue light sensed by the first and second photodiodes, respectively, and, based at least in part on the value stored in the register set, to read out estimated output signals associated with the first and second estimated signals from the estimation	**"an external data output port"**: parallel port interface 60	**"an external data output port"**: parallel port interface 60

circuit.		

Claim 124	**FIG. 6**	**FIG. 8**
124. (Previously presented) A method of operating a CMOS imager comprising: receiving light in an array of pixels, wherein the array of pixels is disposed on a semiconductor substrate, and wherein the array of pixels includes a red pixel to provide a red pixel signal to indicate an amount of red light sensed by the red pixel, a green pixel to provide a green pixel signal to indicate an amount of green light sensed by the green pixel, and a blue pixel to provide a blue pixel signal to indicate an amount of blue light sensed by the blue pixel;	**"an array of pixels"**: See claim 65.	**"array of pixels"**: Same as FIG. 6.
performing correlated double sampling and analog-to-digital conversion on a group of pixel signals using at least M analog processing circuits, wherein the analog processing circuits are disposed on the semiconductor substrate and coupled to receive pixel signals from the array, and wherein each of the analog processing circuits is coupled to a respective one of at least M signal lines from a column decoder;	By operation of analog conditioning circuitry 54, with M=1.	By operation of analog conditioning circuitry 95, with M=3.
providing the group of pixel signals to an interpolator, wherein the interpolator is disposed on the semiconductor substrate, and wherein the group of pixel signals are associated with a group of pixels of the array having M rows of pixels and N columns of pixels, estimating, using the interpolator, an amount of light of first and second colors, received but not sensed by a target pixel, using selected pixel signals within the group of pixel signals associated with pixels that sense light of the first and second colors;	By operation of interpolator 58, with M=1.	By operation of interpolator 90, with M=3.
programming a writable and readable register set to store at least one value to affect an output of interpolated pixel signals, wherein the register set is disposed on the semiconductor substrate and is accessible via an external interface; and	**"a writable and readable register set"**: Within I/O Interface 76. See [0037]. **"to store at least one value to affect an output of interpolated pixel signals"**: The registers of I/O	**"a writable and readable register set"**: Within I/O Interface 76, which is part of interface 60. See [0037]. **"to store at least one value to affect an output of interpolated pixel signals"**: The

	Interface 76 store multiplier gain values. See [0037]. **"accessible via an external interface"**: Control circuit 62 and/or I/O Interface 76.	registers of I/O Interface 76 store multiplier gain values. See [0037]. **"accessible via an external interface"**: Control circuit 93 and/or "to interface 60" at lower right of FIG. 8, which includes I/O Interface 76.
outputting, through an external data output port, first output signals associated with the red, green, and blue pixel signals, and, in accordance with the at least one value to be stored in the register set, second output signals associated with the amount of light of the first and second colors estimated by the interpolator to be received but not sensed by the target pixel.	By operation of analog conditioning circuitry 58, through parallel port interface 60.	By operation of analog conditioning circuitry 95, through parallel port interface 60.

Claim 136	**FIG. 6**	**FIG. 8**
136. (Previously presented) A method of operating a system comprising: writing a value to a writable and readable register set via an external programming interface, wherein the register set is disposed on a semiconductor substrate and coupled via an external input-output port to the external programming interface;	See claim 93.	See claim 93.
receiving light in an array of photodiodes, wherein the array of photodiodes is disposed on the semiconductor substrate, and wherein the array of photodiodes includes a first photodiode to provide a first signal to indicate an amount of red light sensed by the first photodiode, and a second photodiode to provide a second signal to indicate an amount of blue light sensed by the second photodiode;	See claim 93.	See claim 93.
providing a group of signals to an estimation circuit disposed on the semiconductor substrate, wherein the group of signals is associated with a group of photodiodes of the array that sense red and blue light;	See claim 93.	See claim 93.

estimating, using the estimation circuit and the group of signals, an amount of red and blue light received by a pixel having a photodiode configured to sense green light, and providing first and second estimated signals to indicate the amount of the red and blue light, respectively, estimated to be received by the pixel; and	See claim 93.	See claim 93.
outputting, using an external data output port, the first output signals associated with the first and second signals that indicate the amount of red and blue light sensed by the first and second photodiodes, respectively, and, based at least in part on the value stored in the register set, estimated output signals associated with the first and second estimated signals from the estimation circuit.	See claim 93.	See claim 93.

The pending claims still being drawn to the embodiment of FIG. 6 (in addition to FIG. 8), Applicant submits that the claims are not simply drawn to a non-elected invention. Reconsideration and withdrawal of the rejection is respectfully requested.

Summary

As it is believed that all of the rejections set forth in the Official Action have been fully met, favorable reconsideration and allowance are earnestly solicited.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he/she telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

Dated: October 21, 2010

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